AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip ~~having a central circuit area at which a high noise resistivity circuit is formed, a peripheral circuit area surrounding the central circuit area, and a low noise resistivity circuit being formed in the peripheral circuit area;~~

a second semiconductor chip which is mounted on ~~the central circuit area of~~ the first semiconductor chip;

a first electrode group which is ~~formed~~ located on ~~an area between the central circuit area and the peripheral circuit area of~~ the first semiconductor chip so as to be arranged along an outer periphery of the second semiconductor chip;

a second electrode group which is ~~formed~~ located on ~~an outer area of the peripheral circuit area of~~ the first semiconductor chip so as to be arranged along an outer periphery of the first semiconductor chip, wherein the second electrode group surrounds the first electrode group;

a third electrode group which is ~~formed~~ located on the second semiconductor chip;

a plurality of first wires for electrically connecting the first electrode group and the third electrode group to each other; and

external connection terminals which are located around the first semiconductor chip and electrically connected to the second electrode group,

wherein the first semiconductor chip has a first circuit area on which the second semiconductor chip is mounted and a second circuit area which is positioned between the first electrode group and the second electrode group, and wherein the second circuit area includes a circuit which is subject to noise therein.

2. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip having a first circuit element region ~~at which a high noise resistivity circuit is formed,~~ and a second circuit element region ~~at which a low noise resistivity circuit is formed~~ which is apart from the first circuit element region,

and further having an intermediate region which is positioned between the first circuit element region and ~~an outer periphery~~ the second circuit element region, wherein the second circuit element region includes a circuit which is subject to noise therein;

a plurality of first electrodes which are ~~formed~~ located on the first semiconductor chip ~~and arranged in a region between the first circuit element region and the second circuit element region~~;

a plurality of second electrodes which are ~~formed~~ located on the first semiconductor chip and ~~arranged in a region~~ between the second circuit element region and ~~the~~ an outer periphery of the first semiconductor chip, so that the second circuit element region is positioned between the first electrodes and the second electrodes;

a second semiconductor chip which is mounted in the first circuit element region of the first semiconductor chip;

a plurality of third electrodes which are ~~formed~~ located on the second semiconductor chip;

a plurality of first wires ~~for~~ which electrically ~~connecting~~ connects the first electrodes and the third electrodes to each other; and

external connection terminals which are electrically connected to the second electrodes, wherein the external connection terminals are located along the outer periphery of the first semiconductor chip so that the second electrodes are positioned between the send circuit element region and the external connection terminals.

3. (Original) The semiconductor device according to claim 1, wherein:

the external connection terminals are conductive leads;

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance; and

the second electrode group and the leads are electrically connected to each other by a plurality of second wires.

4. (Original) The semiconductor device according to claim 1, wherein a size of the second semiconductor chip is smaller than that of the first semiconductor chip.

5. (Original) The semiconductor device according to claim 1, wherein the first semiconductor chip and the second semiconductor chip are sealed with a resin.

6. (Original) The semiconductor device according to claim 1, wherein:

the external connection terminals are conductive leads;

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance;

the second electrode group and the leads are electrically connected to each other by a plurality of second wires;

the first semiconductor chip and the second semiconductor chip are sealed with a resin; and

the first wires and the second wires are sealed with the resin.

7. (Original) The semiconductor device according to claim 1, wherein the first semiconductor chip is formed on a support.

8. (Currently Amended) The semiconductor device according to claim 1, wherein the first electrode group and the second electrode group are ~~formed~~ located along sides of the outer periphery of the first semiconductor device.

9. (Currently Amended) The semiconductor device according to claim 1, wherein the third electrode group is ~~formed~~ located along ~~an~~ the outer periphery of the second semiconductor chip.

10. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip having a ~~central~~ first circuit area ~~on which a high noise resistivity circuit is formed~~, a ~~peripheral~~ second circuit area surrounding the ~~central~~ first circuit area, ~~on which a low noise resistivity circuit is formed,~~ a first electrode area ~~located~~ positioned between the ~~central~~ first circuit area and the ~~peripheral~~ second circuit area so as to surround the first circuit area, and a second

electrode area ~~located~~ positioned at outside of the ~~peripheral~~ second circuit area so as to surround the second circuit area, wherein the second circuit area includes a circuit which is subject to noise therein;

a second semiconductor chip mounted on the ~~central~~ first circuit area of the first semiconductor chip;

a plurality of first electrodes ~~formed~~ located on the first electrode area of the first semiconductor chip;

a plurality of second electrodes ~~formed~~ located on the second electrode area of the first semiconductor chip;

a plurality of third electrodes ~~formed~~ located on the second semiconductor chip;

a plurality of electrical connections for electrically connecting the first electrodes and the third electrodes, respectively; and

a plurality of external connection terminals electrically connected to the second electrodes, respectively.

11. (Previously Presented) The semiconductor device according to claim 10, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

12. (Currently Amended) The semiconductor device according to claim 10, wherein the ~~low noise resistivity~~ circuit subject to noise includes an analog circuit.

13. (Previously Presented) The semiconductor device according to claim 10, wherein the first and second semiconductor chips are sealed with a resin.

14. (Previously Presented) The semiconductor device according to claim 10, wherein the electrical connections are a plurality of wires.

15. (Previously Presented) The semiconductor device according to claim 10, wherein external connection terminals are electrically connected to the second electrodes by a plurality of wires.

16. (Previously Presented) The semiconductor device according to claim 1, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

17. (Currently Amended) The semiconductor device according to claim 1, wherein the ~~low noise resistivity~~ circuit subject to noise includes an analog circuit.

18. (Previously Presented) The semiconductor device according to claim 2, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

19. (Currently Amended) The semiconductor device according to claim 2, wherein the ~~low noise resistivity~~ circuit subject to noise includes an analog circuit.

20. (Previously Presented) The semiconductor device according to claim 2, wherein the first and second semiconductor chips are sealed with a resin.